CLAIMS

What is claimed is:

1. A system for extracting a threshold voltage, comprising:

a first MOSFET stage including an input operative to receive a first input current, and a gate node electrically coupled to the input thereof;

a second MOSFET stage including an input operative to receive a second input current and a gate node; and

a voltage divider coupled between the input of the second MOSFET stage and the gate node of the first MOSFET stage, the voltage divider also having an intermediate output node coupled to the gate node of the second MOSFET stage, such that an output voltage at the input of the second MOSFET stage is approximately equal to the threshold voltage for at least one of the first and second MOSFET stages.

2. The system of claim 1, the first MOSFET stage further comprising a floating gate MOSFET having a drain that defines the input of the first MOSFET stage and a gate that defines the gate node of the first MOSFET stage, the floating gate MOSFET of the first MOSFET stage operating in a saturation region thereof.

3. The system of claim 2, the second MOSFET stage further comprising a floating gate MOSFET having a drain that defines the input of the second MOSFET stage and a gate that defines the gate node of the second MOSFET stage, the floating gate MOSFET of the second MOSFET stage operating in a saturation region thereof.

4. The system of claim 3, the first and second input currents being proportional to each other.

5. The system of claim 4, the first input current being approximately four times the second input current.

6. The system of claim 4, the first input current and the second input current being functionally related to each other according to the scaling of the respective MOSFETs of the first and second MOSFET stages.

7. The system of claim 3, each of the MOSFETs further comprising a respective PMOS transistor.

8. The system of claim 3, each of the MOSFET further comprising a respective NMOS transistor.

9. The system of claim 1, the voltage divider further comprising a first capacitor connected with a second capacitor in series between the input of the second MOSFET stage and the gate node of the first MOSFET stage, a node between the first and second capacitors defining the intermediate output node that has a voltage functionally related to capacitances of the first and second capacitors.

10. The system of claim 9, the first capacitor having a capacitance substantially equal to the second capacitor.

11. The system of claim 9, the first and second capacitors having respective capacitances that are greater than parasitic gate capacitance associated with the second MOSFET stage.

12. The system of claim 1 defining a first system for extracting a threshold voltage, further comprising a second system for extracting a threshold voltage coupled to the first system for extracting a threshold voltage to provide a stacked threshold voltage extraction system having an output that is an integer multiple of the threshold voltage.

13. The system of claim 1 in combination with a capacitor multiplier system, the combination comprising:

the capacitor multiplier including a first input that receives the output voltage at the input of the second MOSFET stage and a second input that receives a bias current, such that a startup offset for the capacitor multiplier is mitigated when the bias current is applied to the second input.

14. The combination of claim 13, the capacitor multiplier further comprising:

first and second stages coupled together at a common node, the first input of the capacitor multiplier being associated with the common node so that a voltage approximately equal to the threshold voltage is at the common node; and

a feedback capacitor coupled between an output of the capacitor multiplier and the second input of the capacitor multiplier.

15. The combination of claim 14, the first input current and the second input current having values proportional to each other.

16. A system for extracting a threshold voltage, comprising:

a first MOSFET having a drain connected to receive a first input current, a gate electrically coupled to the drain, and a source coupled to a reference potential;

a second MOSFET having a gate, source and drain, the drain being connected to receive a second input current, the source being coupled to the reference potential;

a first part of a voltage divider being coupled between the gate of the first MOSFET and the gate of the second MOSFET;

a second part of the voltage divider being coupled between the gate and the drain of the second MOSFET, such that an output voltage at drain of the second MOSFET is approximately equal to the threshold voltage for at least one of the first and second MOSFETs.

17. The system of claim 16, the first and second input currents being proportional to each other.

18. The system of claim 17, the first input current being approximately four times the second input current.

19. The system of claim 16, the first and second input currents being functionally related to each other according to the scaling of the respective first and second MOSFETs.

20. The system of claim 16, the first and second parts of the voltage divider comprising first and second capacitors.

21. The system of claim 20, the first capacitor having a capacitance substantially equal to that of the second capacitor.

22. The system of claim 21, the first and second capacitors having respective capacitances that are greater than a parasitic gate capacitance associated with the second MOSFET.

23. The system of claim 16, each of the first and second MOSFETs being a respective PMOS transistor.

24. The system of claim 16, each of the first and second MOSFETs being a respective NMOS transistor.

25. The system of claim 16 defining a first system for extracting a threshold voltage and further comprising a second system for extracting a threshold voltage coupled to the first system for extracting a threshold voltage to provide a stacked threshold voltage extraction system having an output that approximates an integer multiple of the threshold voltage.

26. The system of claim 16 in combination with a capacitor multiplier circuit, the combination comprising:

the capacitor multiplier circuit comprising first and second amplifier stages coupled together at a common node, the first stage having a first input that receives a bias current, and an AC feedback network coupled between an output of the second stage of the capacitor multiplier circuit, the output of the second stage of the capacitor multiplier circuit being coupled to the common node; and

the output voltage from the voltage extraction system being applied to the capacitor multiplier so that voltage approximately equal to the threshold voltage is at the common node, such that a startup offset for the capacitor multiplier circuit is mitigated as the bias current is applied to the first input of the capacitor multiplier circuit.

27. A capacitor multiplier system, comprising:

a threshold voltage extraction system that provides an output having a value functionally related to a threshold voltage; and

the capacitor multiplier circuit comprising a first and second stages coupled together at a common gate node, the first stage having a first input that receives an input current, a feedback capacitor being coupled between an output of the second stage of the capacitor multiplier circuit and the first input, the output from the threshold voltage extraction system being provided to a second input of the capacitor multiplier circuit that is operatively connected with the common gate node, such that the threshold voltage is provided to at the common gate node and a startup offset for the capacitor multiplier circuit is mitigated as the input current is applied to the first input.

28. The system of claim 27, the voltage extraction system further comprising a first MOSFET stage coupled to a second MOSFET stage, the first MOSFET stage operative to receive a first input current, the second MOSFET stage having an input operative to receive a second input current, which is proportional to the first input current, the input of the second MOSFET stage defining the output of the voltage extraction.

29. The system of claim 28, further comprising a voltage divider coupled between the input of the second MOSFET stage and a gate node of the first MOSFET stage, the voltage divider also having an intermediate output node coupled to a gate node of the second MOSFET stage, such that a voltage at the input of the second MOSFET stage is approximately equal to a threshold voltage for at least one of the first and second MOSFET stages of the voltage extraction system.

30. The system of claim 27, the voltage extraction system further comprising a plurality of stacked voltage extractors coupled in series so that the output of the voltage extraction system is approximately n times the threshold voltage, where n is an integer greater than zero.

31. A method for extracting a threshold voltage for a MOSFET device having a gate, source and drain, the method comprising:

connecting gates of first and second stages through a first part of a voltage divider, each stage including a respective MOSFET device;

saturating the MOSFET device of the first stage;

providing bias current to an input of the first stage;

providing bias current to an input of the second stage, the input of the second stage being connected to the gate of the second stage through a second part of the voltage divider;

saturating the MOSFET device of the second stage, such that a voltage at the input of the second stage corresponds to the threshold voltage.

32. The method of claim 31, the bias current to the input of the first stage being proportional to the bias current to the input of the second stage.

33. The method of claim 32, further comprising providing the voltage at the input of the second stage to an input of a capacitor multiplier, such that the threshold voltage is applied to an internal node of the capacitor multiplier and a startup offset of the capacitor multiplier is mitigated.